Efficient Design of Conservative Logic Based Sequential Circuits

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Abstract—This paper deals with the testable design of conservative logic based sequential circuits by using two test vectors. The conservative logic based sequential circuits are built from the reversible gates. ThisReversible or information lossless circuits have extensive applications in quantum computing, optical computing, as well as ultra-low power VLSI circuits.Theoptimized designs of reversible D Latch,Reversible negative enable D latch,Master slave Flip-Flop,Double edge triggered Flip-Flops and its application circuits like reversible universal shift registers, four bit binary counter are proposed.This proposed design can identify any stuck-at-fault in the circuits and this proposed circuit is efficient than the conventional circuit designed using classical gate in terms of number of gate count,delay in the circuit,garbageoutput, power dissipation and testability.Thisproposeddesign canidentify any stuck-at-fault in the circuits.

Index Terms— Conservative logic, Fredkin gate, garbage output, reversible logic, Test vector.

1. INTRODUCTION

Conservative logic based circuits does not lose any information and it exhibit the property that there will be one to one mapping between the input and the output so the circuits designed using conservative logic reversible gates are lossless.Landauer[1] have proved that if the operation is performed in irreversible manner by using conventional gates KTln2 Joules of heat energy would dissipate for each 1 bit of information lost and also fan-out problem occurs. Where K is the Boltzmann's constant and T is the absolute temperature where the computation is performed. From the thermodynamic point of view if the computation is performed by using conservative logic based reversible gates KTln2 Joules of heat energy would not dissipate[2] and also fan-out problem does not occurs. There are applications like emerging Nanotechnologies, quantum-.cellular automata computing, optical computing and in ultra-low power VLSI circuits were reversible circuits are used.

An $N \times N$ (N inputs and N outputs) conservative logic based reversible gate can be represented in the vector form as $I_V = I_1, I_2, I_3, I_4 \ldots \ldots \ldots I_N$ and $O_V = O_1, O_2, O_3, O_4 \ldots \ldots \ldots O_N$ .where I_V and O_V represent input and output vectors, respectively. Classical logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states but the reversible gates like Fredkin gate, Toffoligate, Feymengate, Peres gate have the property that the input vector can be recovered from the output vector because they do not lose any information.Unwanted or unused output of a reversiblegate is known as Garbage Output. In other words, the outputs which are needed only to maintain reversible logic are called garbage outputs.

1.1 Conservative Logic Based Fredkin Gate

The Fredkin gate is universal, so that any logical or arithmetic operation can be done by Fredkin gate. For 3*3 Fredkin gate shown in Fig.1 the input vector for fredkin gate and output are defined as $I_V = (A, B, C)$

$O_V = (P = A, Q = \overline{A}B + AC, R = AB + \overline{A}C)$ The truth table of fredkin gate is illustrated in[11]
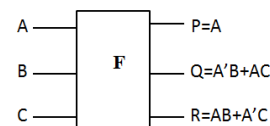

Fig.1. Fredkin gate

1.2 Conservative Logic Based Feymen Gate

For 2*2 Feymen gate shown in Fig.2 the input vector and output vector for Feymen gate are defined as $I_V = (A, B)$ and $O_V = (P = A, Q = A \oplus B)$ .The truth table of Feymen gate is illustrated in[11].
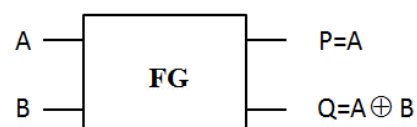

Fig. 2. Feymen gate

1.3 Related Work

The research on conservative reversible logic is expanding towards both the design,synthesis and testing.Several researches have proposed reversible circuits in terms of garbage output,number of gate,power dissipation in[3].The online testing of reversible decoder circuit is addressed in the paper[3].In this paper we propose the novel design of reversible sequential circuits which is testable using only two test vectors.

2. DESIGN OF TESTABLE REVERSIBLE LATCHES

Reversible testable D latch has the characteristic equation $Q^+ = D.E + \overline{E}.Q$ .In the proposed architecture E is the enable and it is used instead of clock.By cascading two fredkin gate the D latch is constructed.When the enable is 1 the input D is passed to the output that is $Q^+ = D$,When the enable is zero the output remains in the previous state.This design has two control signals which are C1 and C2.The design can work in two operating modes :(1)Normal mode and (2)Test mode.

(1)Normal mode:In the normal mode as shown in the Fig.3 the control signal C1C2=01.Thus the circuit will do its normal operation.

(2)Test mode(Disrupt the feedback):In the test mode the stuck at 1 and stuck at 0 faults can be found by changing the control signal.Thestruck-at-0 fault is found by giving C1C2=11,thus any struck-at-0 fault in the circuit can be identified. Similarly the stuck-at-1 fault is found by giving C1C2=00,thus any stuck-at-1 fault in the circuit can be identified.
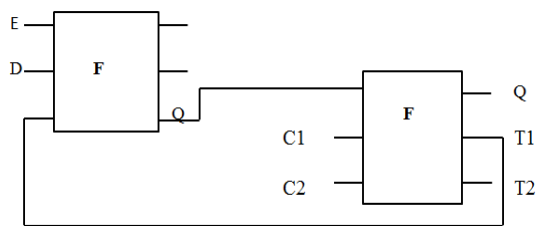

Fig. 3. Design of testable reversible D latch

2.1Design of testable negative enable D latch

Reversible negative testable D latch has the characteristic equation $Q^+ = D.\overline{E} + E.Q$ .In the proposed architecture E is the enable and it is used instead of clock.By cascading two fredkin gate the D latch is constructed.This proposed design passes the input to the output only when the enable is 0 otherwise the latch maintains the same state .This design has two control signals which are C1 and C2.The design can work in two operating modes :(1)Normal mode and (2)Test mode.

(1)Normal mode:In the normal mode as shown in the figure the control signal C1C2=01.Thus the circuit will do its normal operation.

(2)Test mode(Disrupt the feedback):In the test mode the stuck at 1 and stuck at 0 faults can be found by changing the control signal.Thestuck-at-0 fault is found by giving C1C2=11,thus any stuck-at-0 fault in the circuit can be identified. Similarly the stuck-at-1 fault is found by giving C1C2=00,thus any stuck-at-1 fault in the circuit can be identified.
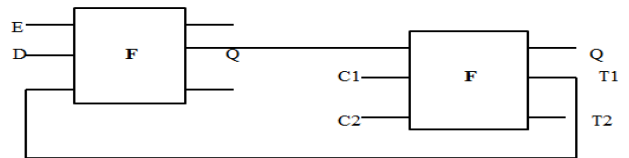

Fig. 4. Design of testable reversible negative enable D latch

3. DESIGN OF TESTABLE REVERSIBLE MASTER SLAVE FLIPFLOP

In the proposed architecture master slave flipflop is designed with the positive enabled D latch as the master and the negative enable D latch as the slave.In the existing method of design of master slave flipflop[6] testing cannot be done,more over the proposed design is optimized in terms of gate count,garbage output and number of constant nput and delay when compared with the existing papers.This design has four control signals which are mC1,mC2,sC1,sC2.The design can work in two operating modes :(1)Normal mode and (2)Test mode.

(1)Normal mode:In the normal mode as shown in the Fig.5 the control signal mC1=0,mC2=1,sC1=0,sC2=1.Thus the circuit will do its normal operation.

(2)Test mode(Disrupt the feedback):In the test mode the stuck at 1 and stuck at 0 faults can be found by changing the control signal.The stuck at 0 fault is found by giving mC1=1,mC2=1,sC1=1,sC2=1,thus any stuck-at-0 fault in the circuit can be identified.similarly the stuck-at-1 fault is found by giving mC1=0,mC2=0,sC1=0,sC2=0,thus any struck 1 fault in the circuit can be identified.
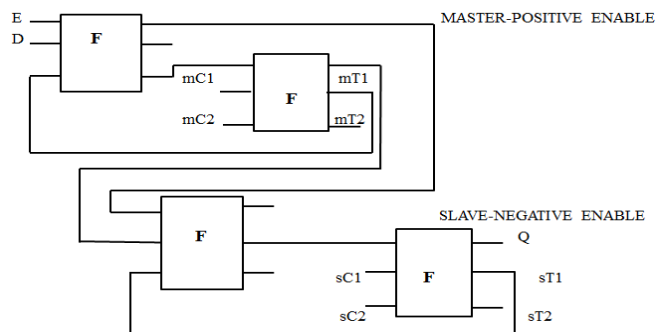

Fig. 5. Design of testable reversible master slave flip-flop

4. DESIGN OF TESTABLE REVERSIBLE DETFLIPFLOP

The double edge triggered flipflop is the sequential circuit which samples and stores the input data at both the positive or rising and negative or falling edge of the clock cycles.In the master slave flipflop,when clock is high the master passes the input while the slave remains in the previous state and when the clock is low the master latch remains in the storage and the slave passes the output of the master to the output.Thus the master salve flipflop does not sample at both the positive and negative edge of the clock cycle.

Thus the DET filpflop using reversible concept is proposed for sampling and storing the data at both the edge of the clock cycle.Thus the frequency of DET filpflop is reduced to half of the master slave flipflop.Thus for the low power applicatons this circuits can be used because frequency is proportional to the power.

In the proposed design DETflipflop is designed by placing a positive enabled and neative enable D latch in parallel as shown in figure.In the proposed design pc1,pc2,nc1,nc2 are the four control signals.The design can work in two operating modes :(1)Normal mode and (2)Test mode.

(1)Normal mode:In the normal mode as shown in the Fig.6 the control signal pC1=0,pC2=1,nC1=0,nC2=1.Thus the circuit will do its normal operation.

(2)Test mode(Disrupt the feedback):In the test mode the stuck at 1 and stuck at 0 faults can be found by changing the control signal. The stuck at 0 fault is found by giving pC1=1,pC2=1,nC1=1,nC2=1,thus any stuck-at-0 fault in the circuit can be identified. Similarly the stuck-at-1 fault is found by giving pC1=0,nC2=0,pC1=0,nC2=0,thus any struck 1 fault in the circuit can be identified.
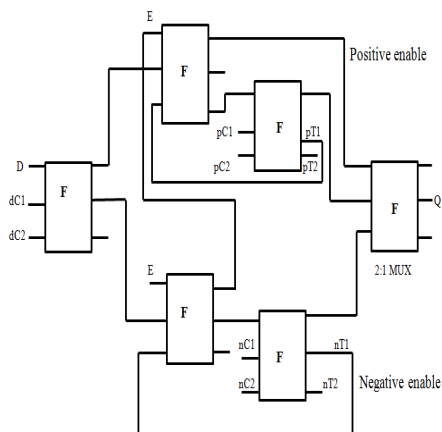
5. APPLICATION OF REVERSIBLE LOGIC FLIP FLOP

Reversible universal shift register is proposed to illustrate the application of reversible flipflop in designing the complex sequential circuits.The universal shift register has the shift as well as the parallel load capabilities.This proposed circuit has right and left shift control signals to perform right and left shift operation respectively. A parallel load control to control the parallel load transfer.figure shows the design of the 4 bit universal reversible shift register.The circuit has 4 reversible D flipflop and four reversible 4:1 multiplexer.reversible Multiplexer is designed using fredkin as shown in the figure.
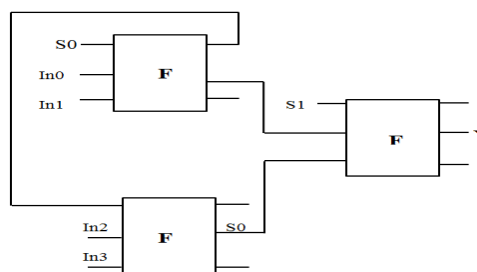

Fig. 7. Design of 4:1 multiplexer

The 4:1 multiplexer has two control signal s0 and s1 which is used to perform left shift,right shift and parallel transfer.The input 0 in the multiplexer is selected when s1s0=00 and thus the present value of the register is applied to the D input of the flipflop.The input 1 in the multiplexer is selected when s1s0=01 and thus the right shift operation takes place.The input 2 in the multiplexer is selected when s1s0=10 and thus the left shift operation takes place.The input 3 in the multiplexer is selected when s1s0=11 and thus the parallel load transfer operation takes place in the universal shift register as shown in the Fig.8
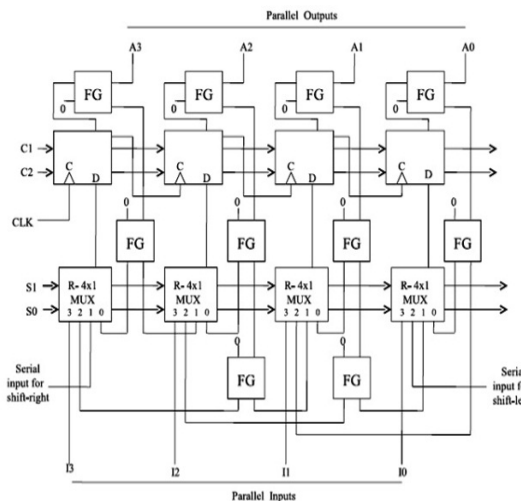

Fig. 6. Design of testable double edge triggeredflip-flop

Fig. 8. Design of reversible universal shift register

TABLE 1:COMPARISON OF PROPOSED REVERSIBLE D LATCH

Master slave flipflop	parameter		
	No of gate	Online testable	No of garbage output
proposed	4	yes	6
Existing[5]	6	no	5
Existing[6]	12	no	14

TABLE 2:COMPARISON OF PROPOSED REVERSIBLE MASTER SLAVEFLIP-FLOP

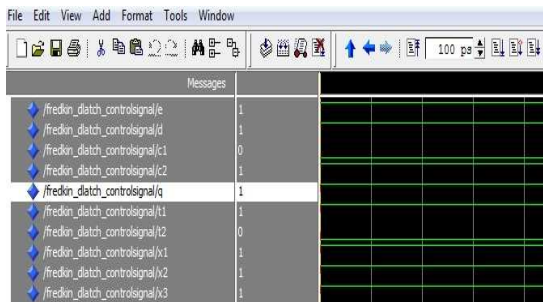| Parameter	Existing [4]	Proposed	Improvement (%)
No of gate	7	4	43
No of constant input	24	4	83
No of garbage output	14	4	71

6.   SIMULATION AND RESULTS

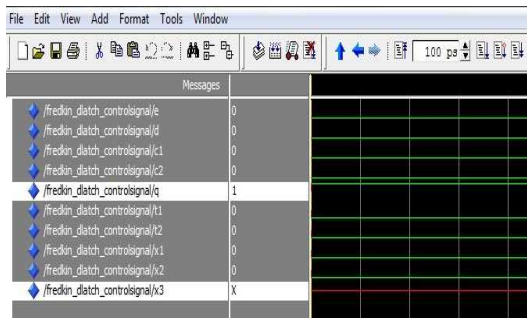Fig. 9.Simulation of testable reversible D latch in normal mode

Fig. 10.Simulation of testable reversible D latch detecting stuck–at-1 fault

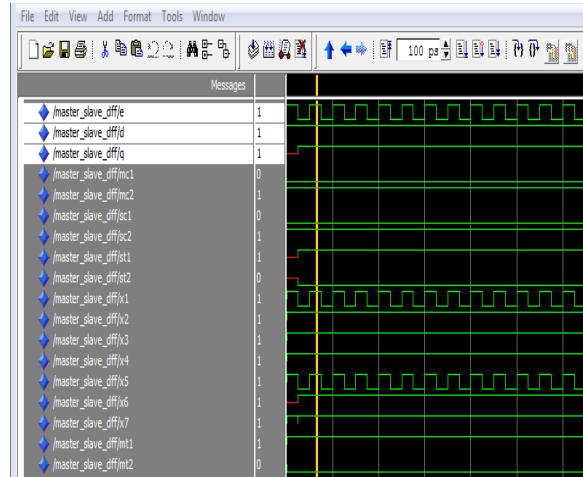
Fig. 11.Simulation of testable master salve flip-flop in normal mode

The simulation result of D latch is shown in figure.9 which act in normal mode by giving the control signal 01.figure.10 shows the same design working in test mode,the circuit detects the stuck-at-1 fault in the pin x3 by giving the control signal as 00 .similarly the simulation result of master slave flipflop working in normal mode is shown in figure.11.
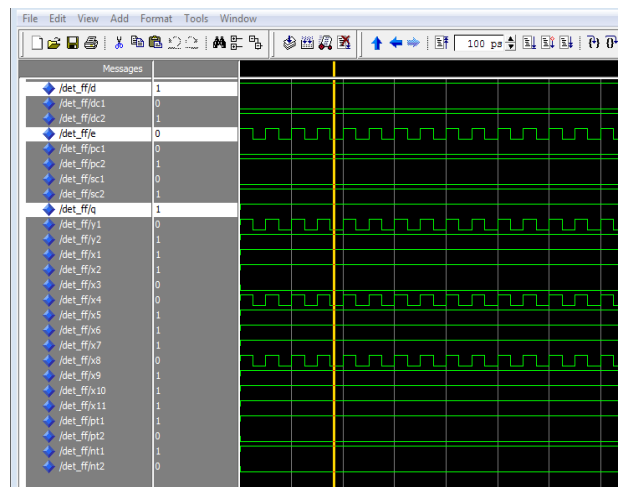

Fig.12. Simulation of testable reversible DET flip-flop in normal mode

The simulation result of reversible DET flipflop is shown in figure.13 which act in normal mode by giving the control signal 01.The same design working in test mode is shown in the figure. 14 which detects the stuck-at-1 fault in the pin x11 by giving the control signal as 11 and also the stuck-at-0 fault can be detected by changing the control signal to 00.
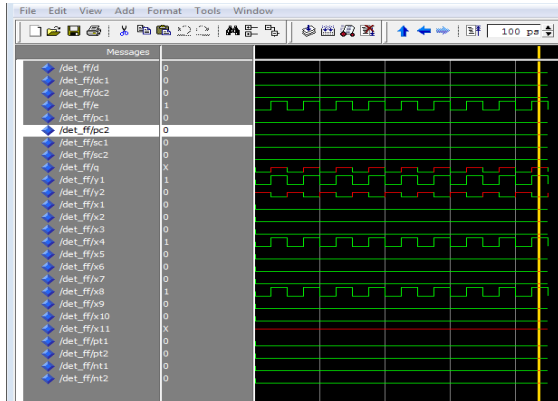
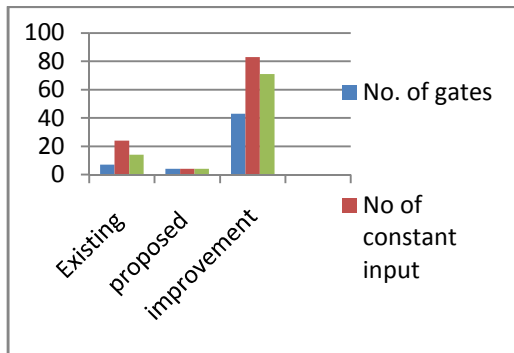Fig. 13.Simulation of testable reversible DET flip-flop detecting stuck-at-0 fault

Fig.14 .Comparison of reversible D latch

The graph shows the comparsion of reversible D latch with existing designs in terms of number of gate,constant input and garbage output.Thus the proposed system provides the good improvement in the result as shown in the figue.14 interms of many parameters.

7. CONCLUSION

The proposed conservative logic based sequential circuit can be testable for any stuck at fault using only two test vectors which are 0s and 1s. Reversible universal shift register is proposed to illustrate the application of reversible flip flop in designing the complex sequential circuit.Thus the main advantage of the proposed circuit is that need of only two test vectors is used to test any sequential circuit..Thus the proposed circuit is efficient than the conventional circuit designed using classical gate in terms of number of gate count,delay,garbageoutput,power dissipation and testability.

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